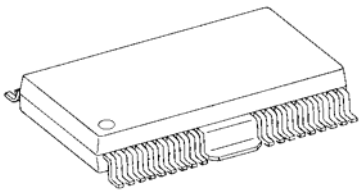
Preliminary TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB6588FG

PWM Sensorless Driver for 3-Phase Full-Wave BLDC Motors

The TB6588FG provides sensorless commutation and PWM current control for 3-phase full-wave BLDC motors. It controls rotation speed by changing a PWM duty cycle by analog voltage.



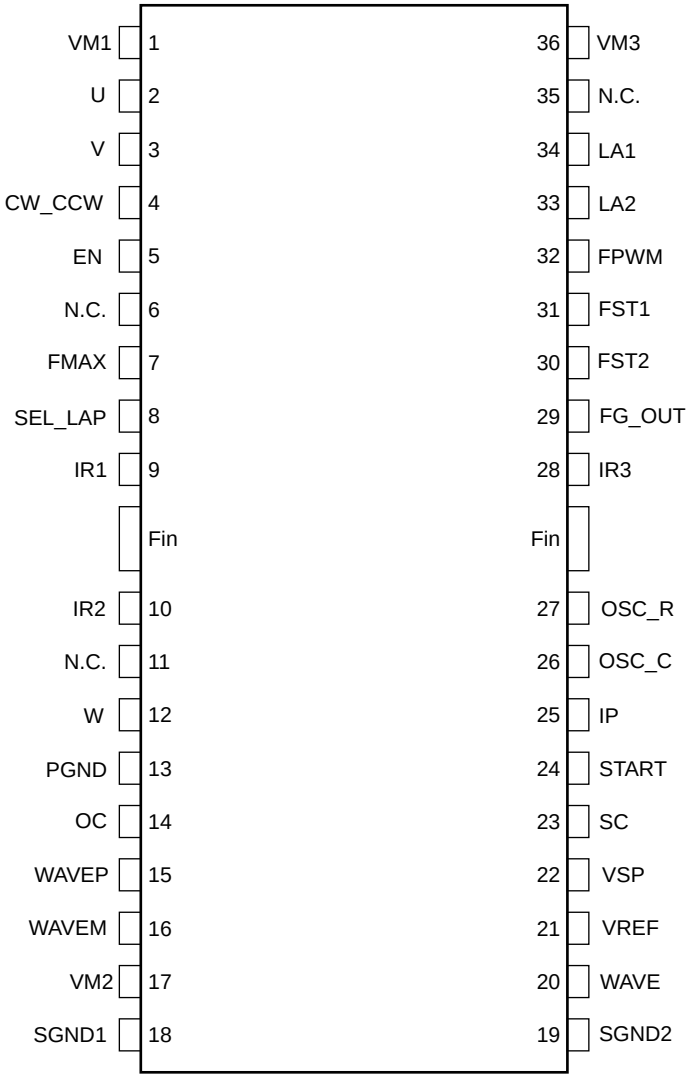
HSOP36-P-450-0.65

Weight: 0.79 g (typ.)

Features

- 3-phase full-wave sensorless drive
- PWM chopper drive
- PWM duty cycle control by analog input (7-bit AD converter)
- Output current: Iout = 2.5 A (max), 1.5 A (typ.)
- Overcurrent protection
- Forward/reverse rotation
- Lead angle control (0°, 7.5°, 15° and 30°)
- Overlap commutation
- Rotation speed detecting signal
- DC excitation mode to improve startup characteristic
- Adjustable DC excitation time and forced commutation time for startup operation
- Forced commutation frequency control capability ($f_{osc}/(6 \times 2^{16})$, $f_{osc}/(6 \times 2^{17})$, $f_{osc}/(6 \times 2^{18})$, $f_{osc}/(6 \times 2^{19})$)

Pin Assignment



Pin Description

Pin No.	Symbol	I/O	Description
-	SGND	—	Signal ground pin
-	SC	I	Connection pin for a capacitor to set a startup commutation time and ramp-up period during duty-cycle operation
-	FPWM	I	PWM frequency select input (This pin has a pull-down resistor.) High : fPWM = f_{osc}/128 Low, Open : fPWM = f_{osc}/256
-	FMAX	I	Set an upper limit of the maximum commutation frequency. (This pin has a pull-up resistor.) High, Open : Maximum commutation frequency fMAX = $f_{osc}/(6 \times 2^8)$ Low : Maximum commutation frequency fMAX = $f_{osc}/(6 \times 2^9)$
-	VSP	I	Duty cycle/motor speed control input (This pin has a pull-up resistor.) $0 \leq VSP \leq V_{AD}$ (L): Output off V_{AD} (L) $\leq VSP \leq V_{AD}$ (H): Set the PWM duty cycle according to the analog input. V_{AD} (H) $\leq VSP \leq$ VREF : Duty cycle = 100% (127/128)
-	CW_CCW	I	Rotation direction input (This pin has a pull-up resistor.) High, Open : Forward rotation (U $\rightarrow$ V $\rightarrow$ W) Low : Reverse rotation (U $\rightarrow$ W $\rightarrow$ V)
-	FG_OUT	O	Rotation speed detect signal output The pin is low at startup or upon a detection of a fault. This pin drives three pulses per rotation (3 ppr) based on the induced voltage in sensorless mode. (In the case of 4-pole motor, 6 pulse output per rotation.)
-	START	O	DC excitation time setting pins When VSP $\geq$ 1 V (typ.), the START pin goes low to start DC excitation. After the IP pin reaches VREF/2, the TB6588FG moves from DC excitation to forced commutation mode.
-	IP	I	
-	OSC_C	—	Connection pin for an oscillator capacitor
-	OSC_R	—	Connection pin for an oscillator resistor
-	LA1	I	Lead angle control input (These pins have pull-up resistors.) LA2: LA1 = High, Open : High, Open = Lead angle of 30° LA2: LA1 = High, Open : Low = Lead angle of 15° LA2: LA1 = Low : High, Open = Lead angle of 7.5° LA2: LA1 = Low : Low = Lead angle of 0°
-	LA2	I	
-	U	O	Phase-U output
-	V	O	Phase-V output
-	W	O	Phase-W output
-	IR	O	Connection pin for an output shunt resistor
-	OC	I	Overcurrent detection input (This pin has a pull-up resistor.) The all PWM output signals are stopped when OC $\geq$ 0.5 (V).
-	WAVE	O	Position signal output Generate a majority logic signal of 3-phase terminal voltage.
-	SEL_LAP	I	Overlap commutation select pin (This pin has a pull-up resistor.) High, Open : 120° commutation Low : Overlap commutation
-	VREF	—	5-V power supply pin
-	WAVEP	I	Position signal input (+)
-	WAVEM	I	Position signal input (–)
-	FST1	I	Forced commutation frequency select pin (These pins have pull-down resistors.) FST2: FST1 = High : High = Forced commutation frequency $f_{ST} = f_{osc}/(6 \times 2^{16})$ FST2: FST1 = High : Low, Open = Forced commutation frequency $f_{ST} = f_{osc}/(6 \times 2^{17})$ FST2: FST1 = Low, Open : High = Forced commutation frequency $f_{ST} = f_{osc}/(6 \times 2^{18})$ FST2: FST1 = Low, Open : Low, Open = Forced commutation frequency $f_{ST} = f_{osc}/(6 \times 2^{19})$
-	FST2	I	
-	VM	—	Motor power supply pin
-	PGND	—	Power ground pin

Pin No.	Symbol	I/O	Description
-	EN	I	Fault protection operation select input (This pin has a pull-up resistor.) High, Open : Protection operation is ON. Low : Protection operation is OFF.

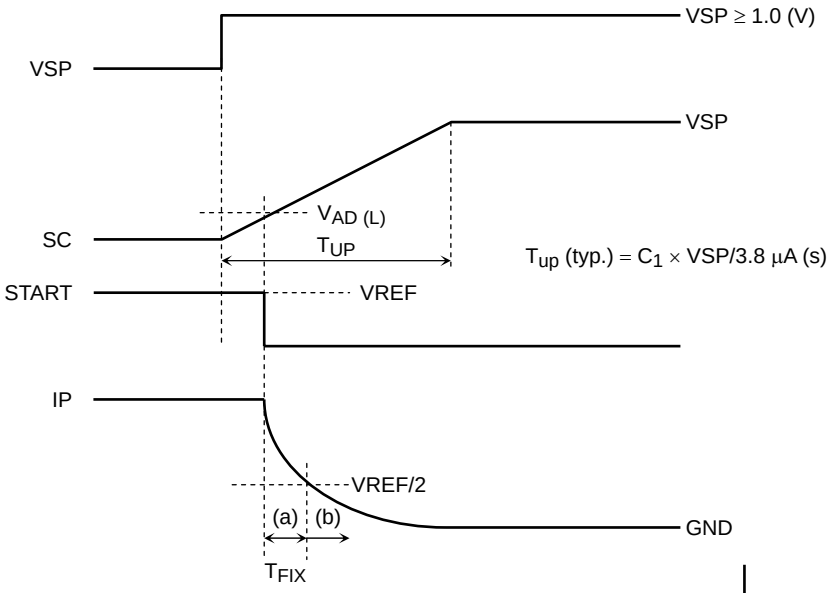
Functional Description

1. Sensorless drive

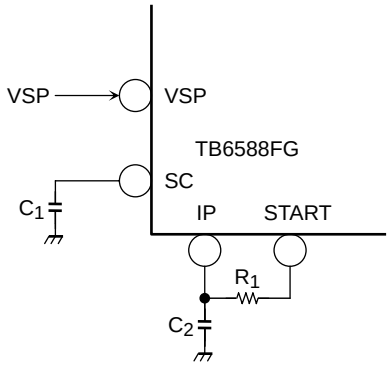
Upon receiving an analog voltage signal input for startup, the rotor is aligned to a known position in DC excitation mode, and then the rotation is started in forced commutation mode by applying a PWM signal to the motor. As the rotor moves, the back-EMF is acquired in each phase of the coil.
When a signal indicating the polarity of each phase terminal voltages including back-EMF is applied to the position signal input, automatic switching occurs from the forced commutation PWM signal to the normal commutation PWM signal based on the position signal input (detected back-EMF) to drive a BLDC motor in sensorless mode.

2. Startup operation

At startup, there is no back-EMF due to the stationary motor, and the motor position cannot be detected in sensorless mode. To avoid this, the TB6588FG rotor is first aligned to a known position in DC excitation mode for a certain period of time, and then the motor is started in forced commutation mode. Each period of DC excitation and forced commutation drives is set with an external capacitor. These time settings vary depending on the motor type and motor loading, so that they should be adjusted experimentally.



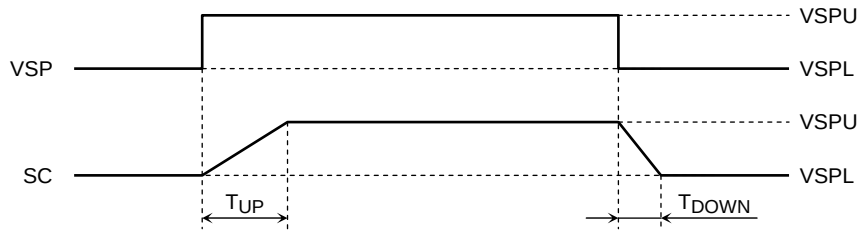
(a): DC excitation time: T_{FIX} (typ.) = 0.69 × C_2 × R_1 (s)
(b): Forced commutation time



The rotor is aligned to a certain position specified in DC excitation mode for the period of (a), during which the IP pin voltage decreases from VREF to VREF/2 level. The time constant for the period is determined by C_2 and R_1. After that, operation mode is switched to forced commutation mode (b) as shown above. The duty cycles for DC excitation and forced commutation modes are determined according to the SC pin voltage. When the rotational frequency exceeds the forced commutation frequency specified with the status of the FST pins, the operation mode is switched to the sensorless mode. The duty cycle for sensorless mode is determined by the VSP value.

3. Operating delay under rotational speed control

Rotation speed of the motor, including rotation startup and stop, is controled by applying the speed command voltage to the VSP pin. However, the operation of the device is actually determined by applied voltage to the SC pin. The voltage on the SC pin is the charging voltage of a capacitor C_1, which is determined by the charging/discharging time of C_1. This induces an operating delay. When the applied voltage on the VSP pin is varied from 1 to 4 V, the operating delay occurs as shown below.



- Charging time of C_1 (when accelerating): T_{UP} (typ.) = C_1 × (VSPU – VSPL)/3.8 μA (s)
- Discharging time of C_1 (when decelerating): T_{DOWN} (typ.) = C_1 × (VSPU – VSPL)/36 μA (s)

Note: When the motor is stopped (VSP < 1 V), the SC pin capacitor C_1 is instantly discharged. (Discharging time of C_1 is the time C_1 is discharged through 2 kΩ (typ.) to GND.)

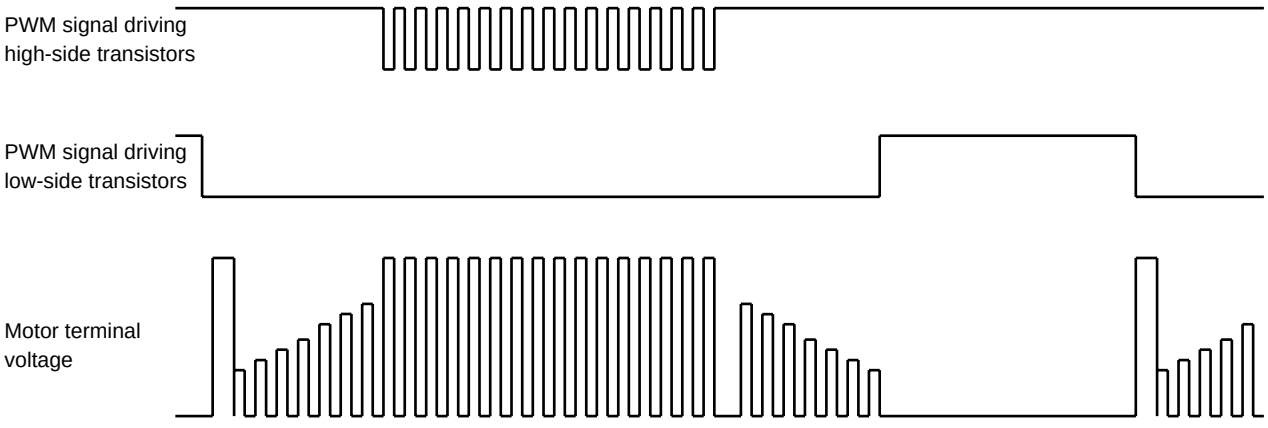
4. Forced commutation frequency

The forced commutation frequency at startup is set as follows.
The optimal frequency varies depending on the motor type and motor loading, so that they must be adjusted experimentally.
The forced commutation frequency is determined by the value of external capacitor and resistor, and also the logic level of FST1 and FST2 pins (These pins have pull-down resistors).

FST2: FST1 = High : High = Forced commutation frequency $f_{ST} = f_{osc}/(6 \times 2^{16})$
FST2: FST1 = High : Low, Open = Forced commutation frequency $f_{ST} = f_{osc}/(6 \times 2^{17})$
FST2: FST1 = Low, Open : High = Forced commutation frequency $f_{ST} = f_{osc}/(6 \times 2^{18})$
FST2: FST1 = Low, Open : Low, Open = Forced commutation frequency $f_{ST} = f_{osc}/(6 \times 2^{19})$

5. PWM frequency

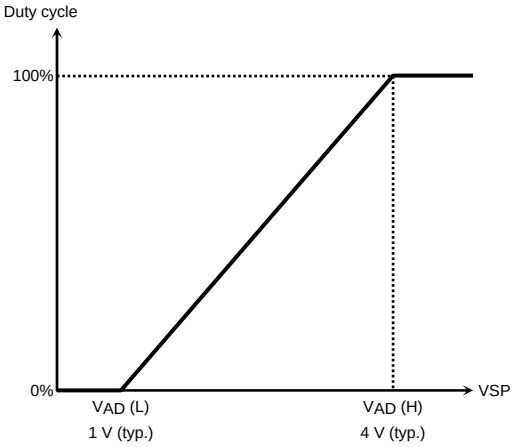
The PWM frequency is determined by the value of external capacitor and resistor, and the logic level of the FPWM pin (This pin has a pull-down resistor).
High : fPWM = $f_{osc}/128$
Low, Open : fPWM = $f_{osc}/256$
The PWM frequency must be sufficiently high, compared to the electrical frequency of the motor. It also must be within the allowable range of switching performance of the driver circuit.



6. Speed control pin (VSP)

An analog voltage applied to the VSP pin is converted by a 7-bit AD converter to control the duty cycle of the PWM.

$0 \leq V_{DUTY} \leq V_{AD}$ (L)
→ Duty cycle = 0%
V_{AD} (L) $\leq V_{DUTY} \leq V_{AD}$ (H)
→ Figure on the right (1/128 to 127/128)
V_{AD} (H) $\leq V_{DUTY} \leq$ VREF
→ Duty cycle = 100% (127/128)



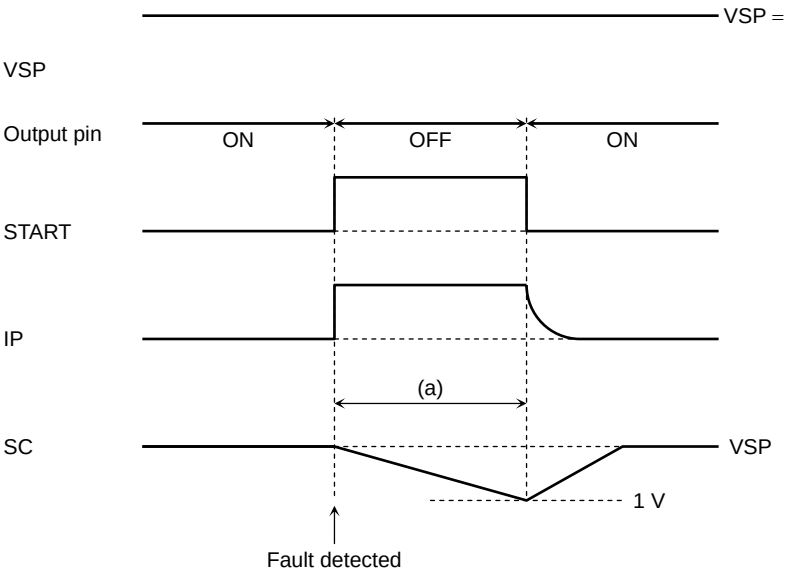
7. Fault protection operation

The logic level of the EN pin determines whether to activate the protection operation.
(This pin has a pull-up resistor.)

High, Open : Protection operation = On
Low : Protection operation = Off

When a signal indicating the following faults is detected at the WAVEP,WAVEM pin, the output transistors are disabled by determining that the motor is in the abnormal state. About one second later, the motor is restarted. This operation is repeated as long as a fault is detected.

- The maximum commutation frequency is exceeded.
- The rotation speed falls below the forced commutation frequency.



When the SC pin capacitor = 0.47 μF and VSP = 4 V

(a): $T_{OFF} = \dfrac{C_{SC} \times (VSP - 1)}{i}$

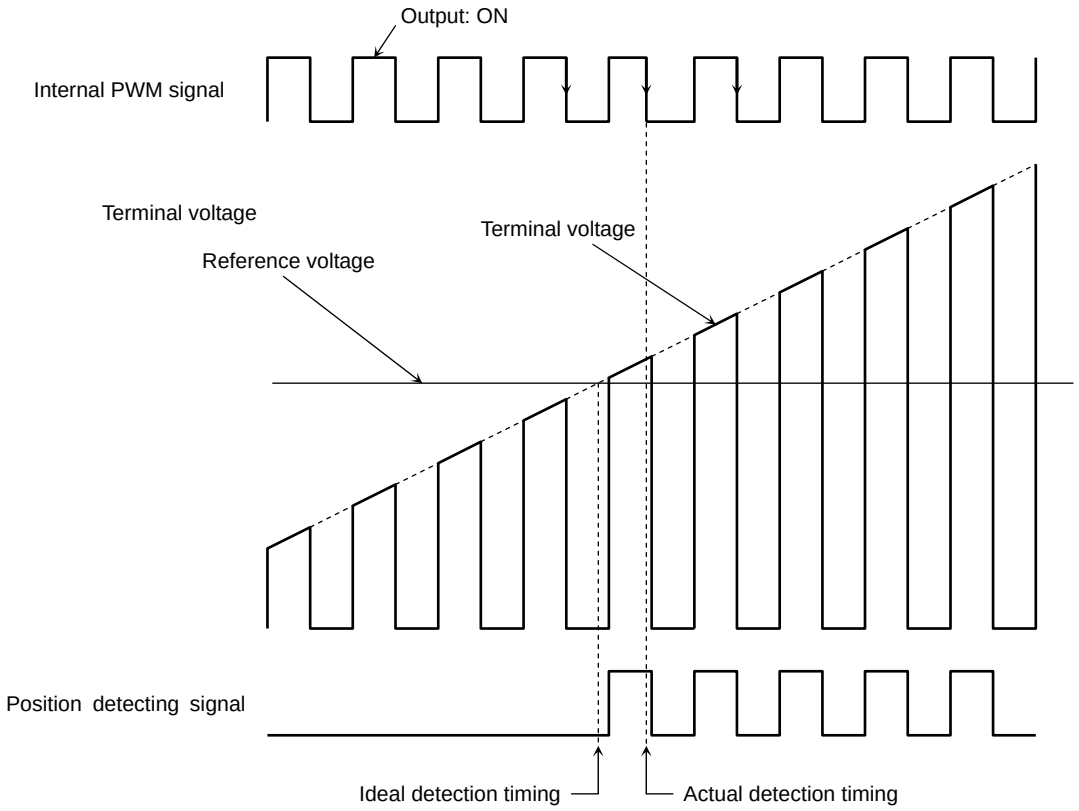
$= \dfrac{0.47\,\mu F \times (4-1)}{1.5\,\mu A}$

= 940 ms (typ.)

8. Motor position detection error

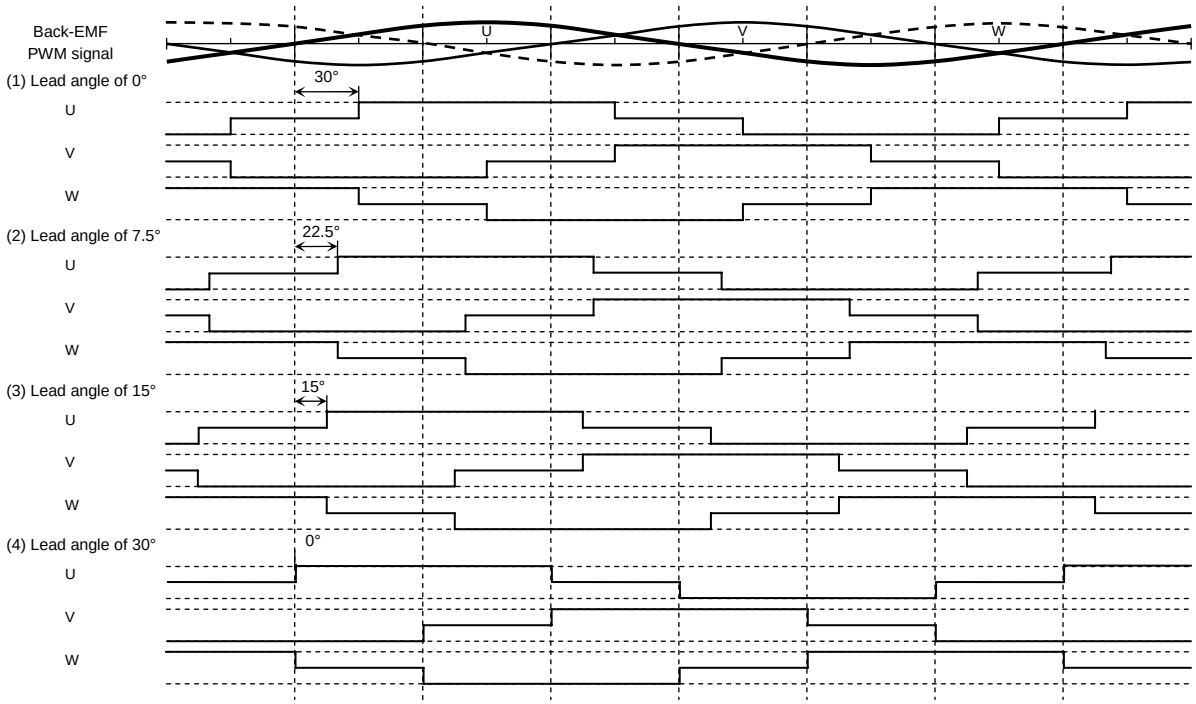
The position detection is synchronized with the PWM signal generated in the IC. Thus, a position detection error related to the PWM signal frequency may occur. Caution is required when the TB6588FG is applied to a high-speed motor.
The detection is performed on the falling edge of the PWM signal. An error is recognized when the terminal voltage exceeds the reference voltage.

Detection lag < $1/f_p$ f_p: PWM frequency = $f_{osc}/256$, fosc/128 f_{osc}: CR (capacitor-resistor) frequency



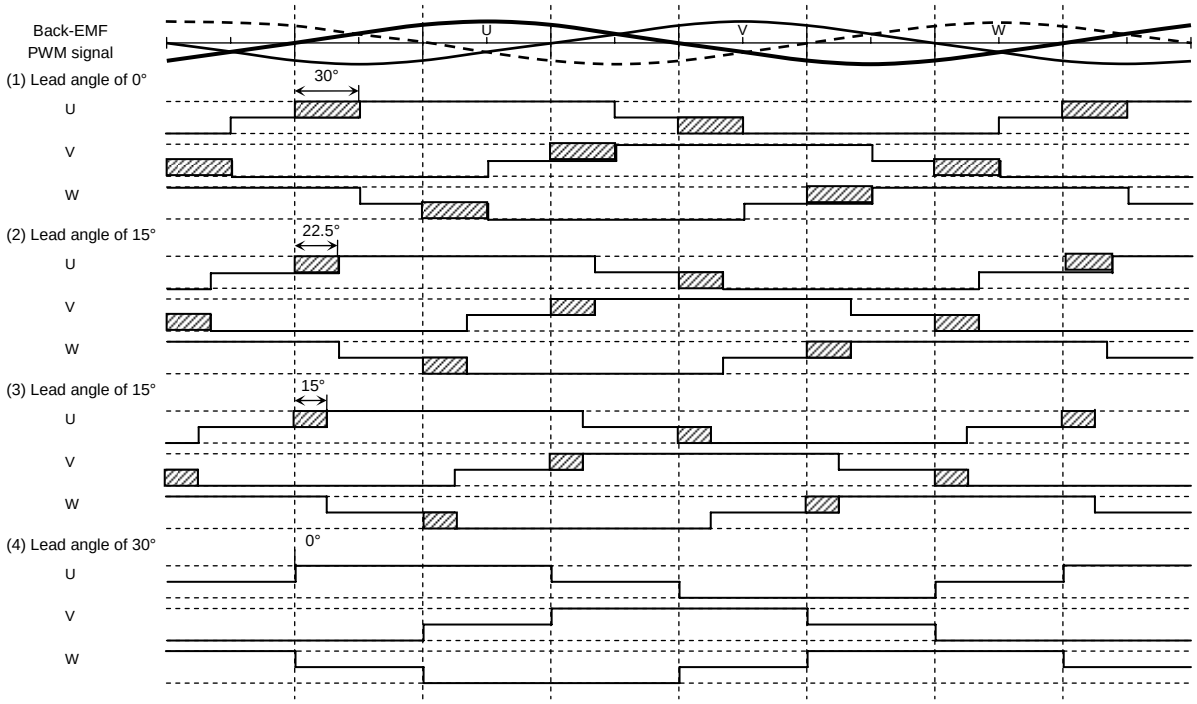
9. Lead angle control

The motor runs with a lead angle of 0° in forced commutation mode at startup. After switching to normal commutation mode, the lead angle is automatically changed to the value set by the LA1 and LA2 pins.



10. Overlap commutation control

When SEL_LAP = High, the TB6588FG is configured to allow for 120° commutation. When SEL_LAP = Low, it is configured to allow for overlap commutation mode. In overlap commutation mode, there occurs an overlap period due to the lengthened commutation time from the zero cross point to the 120° commutation timing upon PWM signal switching as shown in the shaded areas. These periods vary depending on the lead angle setting.



Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	VM	50	V
Input voltage	V_{in}	−0.3 to VREF + 0.3	V
Turn-on signal output current	I_{OUT}	2.5 (Note 1)	A
Power dissipation	P_D	1.4 (Note 2)	W
		3.2 (Note 3)	
Operating temperature	T_{opr}	−30 to 105	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note 1: Output current maybe controlled according to the ambient temperature or a heatsink. The maximum junction temperature should not exceed T_{jmax} = 150°C.

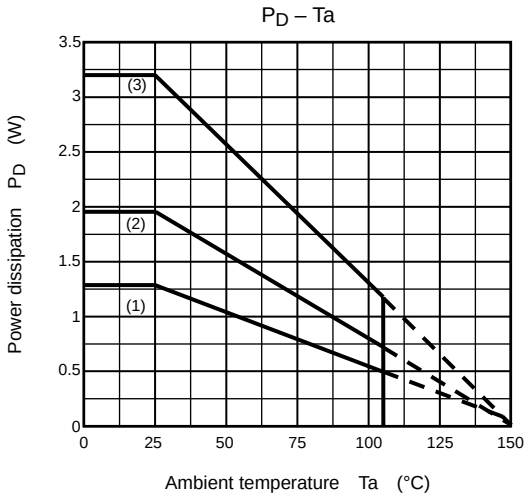
Note 2: Measured for the IC only. (Ta = 25°C)

Note 3: Measured when mounted on the board. (100 × 200 × 1.6 mm, Cu: 50%)

Recommended Operating Conditions (Ta = –30 to 105°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Power supply voltage	VM	10	24	42	V
Input voltage	V_{in}	−0.3	—	VDD + 0.3	V
Oscillation frequency	F_{OSC}	4.0	5.0	6.0	MHz

Package Power Dissipation

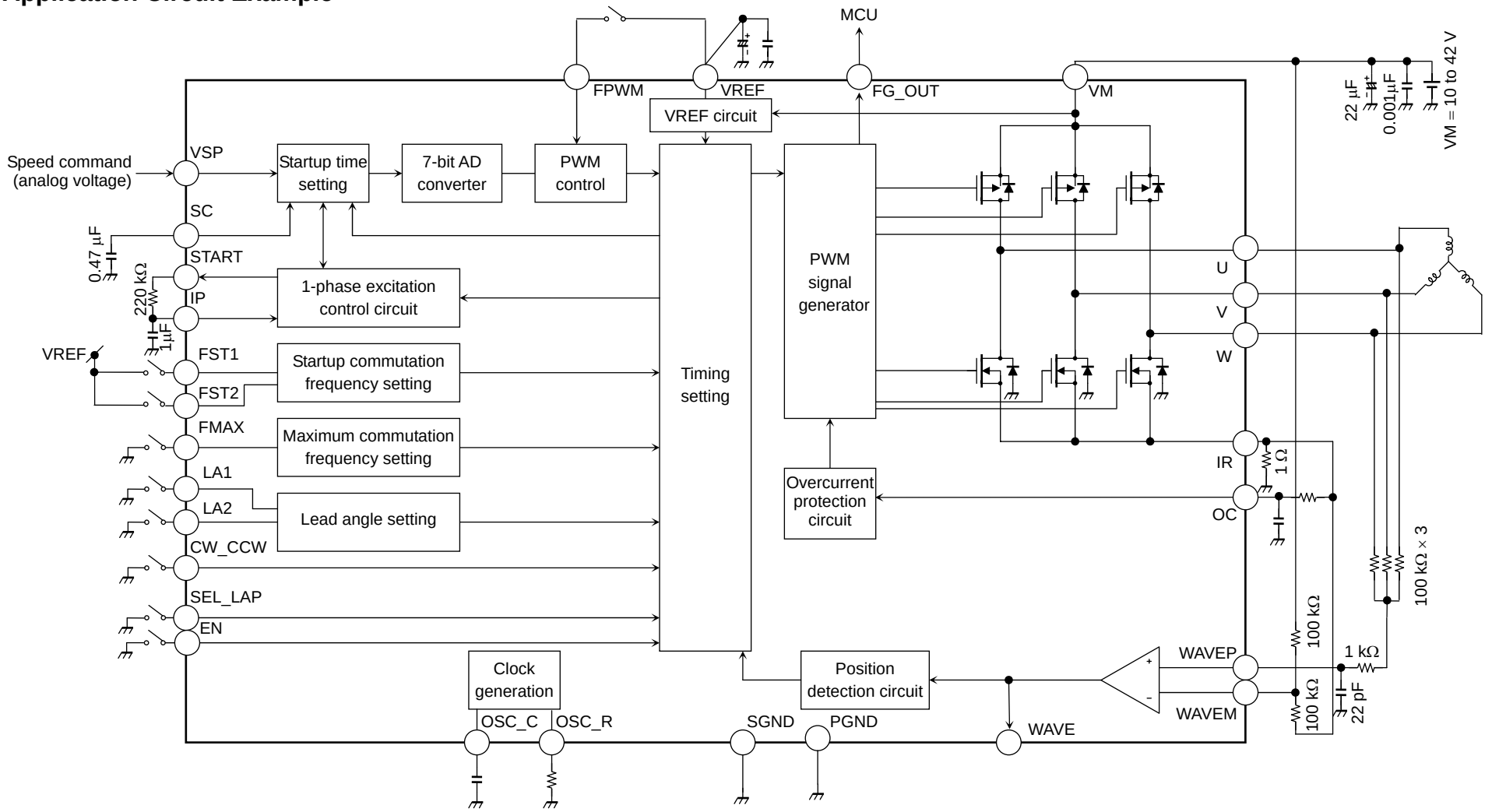


(1) R_{th} (j-a) only (96°C/W)
(2) When mounted on the board (114 mm × 75 mm × 1.6 mm, Cu 20%: 65°C/W)
(3) When mounted on the board (140 mm × 70 mm × 1.6 mm, Cu 50%: 39°C/W)

Electrical Characteristics (Ta = 25°C, VM = 24 V)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Static power supply current at VM	IM	VSP = 0 V, X_{Tin} = H	—	(0.5)	(1)	mA
Dynamic power supply current at VM	$I_{M\ (opr)}$	V_{SP} = 2.5 V, X_{Tin} = 5 MHz, Output Open	—	(1.0)	(2.0)	mA
Input current	I_{IN-1} (H)	V_{IN} = 5V, OC, SEL_LAP,FMAX,EN, CW_CCW,LA1,LA2	—	0	1	μA
	I_{IN-1} (L)	V_{IN} = 0 V, OC,SEL_LAP,FMAX,EN CW_CCW,LA1,LA2	−75	−50	—	
	I_{IN-2} (H)	V_{IN} = 5 V, FST1, FST2, FPWM	—	50	75	
	I_{IN-2} (L)	V_{IN} = 0 V, FST1, FST2, FPWM	−1	0	—	
	I_{IN-3} (L)	V_{IN} = 5 V, VSP	—	90	150	
	I_{IN-3} (L)	V_{IN} = 0 V, VSP	−1	0	—	
Input voltage	V_{IN-1} (H)	SEL_LAP, CW_CCW, LA1, LA2, FMAX, FST1, FST2, EN, FPWM	3.5	—	5	V
	V_{IN-1} (L)	SEL_LAP, CW_CCW, LA1, LA2, FMAX, FST1, FST2, EN, FPWM	GND	—	1.5	
Input hysteresis voltage	V_H	IP	—	0.45	—	V
FG output voltage	V_O (H)	I_{OH} = −0.5 mA FG_OUT	4.5	—	VREF	V
	V_O (L)	I_{OL} = 0.5 mA FG_OUT	GND	—	0.5	
Output ON-resistance	R_{ON} (H)	I_{OUT} = 1.5 A U, V, W	—	(0.3)	(0.35)	Ω
	R_{ON} (L)	I_{OUT} = −1.5 A U, V, W	—	(0.2)	(0.25)	
Output leak current	I_L (H)	V_{OUT} = 0 V	—	0	1	μA
	I_L (L)	V_{OUT} = 42 V	—	0	1	
	IFGL (H)	VREF = 5.5 V, V_{OUT} = 0 V FG_OUT	—	0	10	
	IFGL (L)	VREF = 5.5 V, V_{OUT} = 5.5 V FG_OUT	—	0	10	
PWM input voltage	V_{AD} (L)	VSP	0.8	1.0	1.2	V
	V_{AD} (H)		3.8	4.0	4.2	
C_{SC} charge current	I_{SC}	SC	2.6	3.8	5.0	μA
Fault recovery time	T_{OFF}	VSP = 4 V, SC pin = 0.47 μF	—	940	—	ms
Overcurrent detection voltage	V_{OC}	OC	0.46	0.5	0.54	V
PWM oscillating frequency	Fc H (5 M)	FPWM = H, f_{osc} = 5 MHz OSC_C = (100 pF), OSC_R = (20 kΩ)	36	40	44	kHz
	Fc L (5 M)	FPWM = L, f_{osc} = 5 MHz OSC_C = (100 pF), OSC_R = (20 kΩ)	18	20	22	
Overheat protection	TSD	(Reference value)	(150)	165	(180)	°C
	TSDhys	Recovery hysteresis (Reference value)	—	15	—	
VREF output voltage	VREFout	IVREF=-1mA	4.5	5	5.5	V

Application Circuit Example



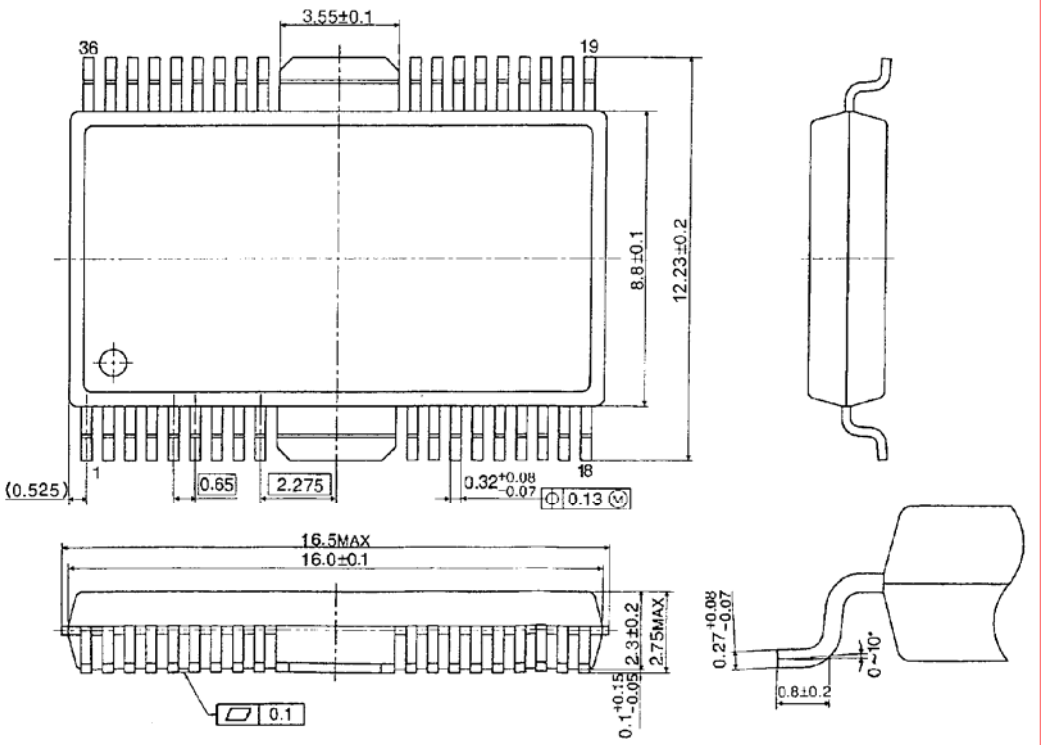
Note 1: Utmost care is necessary in the design of the output, VM, and GND lines since the IC may be destroyed by short-circuiting between outputs, or short-circuiting to VM and GND.

Note 2: The above application circuit including constant values is for reference only. Since each value may vary depending on the motor type, the optimal values must be determined experimentally.

Note 3: Connect a resistor, if necessary, to prevent malfunction due to noise.

Package Dimensions

HSOP36-P-450-0.65 Unit: mm



Weight: 0.79 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

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